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(54) **Semiconductor wafer array.**

(57) A semiconductor wafer array comprising a plurality of wafers (10-18) of semiconductor material. Each of the wafers (10-18) is provided with cone-shaped or pyramid-shaped vias (25). Inserted in each of the vias (25) is a correspondingly shaped wad of electrically conductive compliant material for foaming continuous vertical electrical connections between the wafers (10-18) in the stack. The base of each wad makes connection to a bonding pad (32-37) on the surface (30) of a lower wafer (10-18) as well as to the electrically conductive compliant material in the lower wafer (10-18).

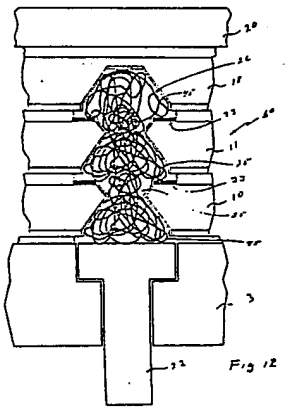

Fig 12

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Fig. 5 is a cross-sectional view of the wafer of Fig. 4 after it has been patterned to expose a square area on the backside of the semiconductor wafer substrate beneath the pads;

Fig. 6 is a cross-sectional view of the wafer of Fig. 5 showing two through-holes provided therein;

Fig. 7 is an enlarged cross-sectional view of one of the vias shown in Fig. 6 after the etch-resistant coating shown in Figs. 4-6 is removed from the center of the ring-shaped pad surrounding the via.

Fig. 8 is a cross-sectional view of the via of Fig. 7 after the sharp edges at the apex of the via are removed;

Fig. 9 is a cross-sectional view of the via of Fig. 8 after its walls have been coated with an electrically insulating layer.

Fig. 10 is a cross-sectional view of the via of Fig. 9 after the etch-resistant coating shown in Figs. 4-9 is removed from the ring-shaped pad.

Fig. 11 is a cross-sectional view of the via of Fig. 10 after a wad of compliant electrically conductive fine wire is inserted therein;

Fig. 12 is an enlarged partial cross-sectional view showing two wafers stacked one on top of another between a dummy wafer and a base plate with the wad of Fig. 11 inserted in each of the vias located therein according to the present invention;

Fig. 13 is an enlarged partial cross-sectional view showing an alternative embodiment of the present invention, comprising electrically conductive compliant elastomeric material;

Fig. 14 is an alternative embodiment of the present invention showing the top of a wad of fine wire compressed onto the pad surrounding the via; and

Fig. 15 is a partial cross-sectional view showing relative dimensions of the vias in the wafers.

Referring to Fig. 1, there is provided in accordance with the present invention a semiconductor wafer array designated generally as 1. In the array 1 there is provided a housing 2 mounted on a base plate 3. In the housing 2 there is provided a plurality of side walls 4, 5 and 6 and a top wall 7. A front wall corresponding to side walls 4-6 is not shown. Located in the housing 2 between the base plate 3 and top wall 7, there is provided a stack of semiconductor wafers 10-18. In the stack of wafers 10-18, the bottom wafer 10 is located adjacent to the base plate 3. The top wafers 18 is located nearest to the top wall 7. Wafer 18 may be a dummy wafer which is used simply for terminating the vertical electrical connecting members and forming an electrical connection with the pads on wafer 17 as will be further described below. On top of wafer 18 between wafer 18 and top wall 17, there is provided a compliant electrically insulating thermally conductive pad 20. Pad 20 is located between the wafer 18 and the top wall 7 to compensate for thermal expansion and contraction of the stack of wafers 10-18 and for conducting heat from the stack of wafers 10-18 to the top wall 7. Extending from the top wall 7 there is provided a plurality of metallic fingers 21. Fingers 21 comprise cooling fins for dissipating heat from the housing 2.

Extending through the base plate 3 there is provided a plurality of electrical pin members 22. Pin members 22 are provided for making electrical contact with electrically conductive compliant material in vias in the stack of wafers 10-18, as will be further described below.

In practice, the base plate 3 comprises insulating material, such as ceramic material, for insulating the pin members 22 from each other, and the side wall members 2 and 4 may comprise a metallic material. The free area within the housing 2 may be filled with a conventional electrically non-conductive gaseous or liquid material to facilitate the dissipation of heat from the housing 2.

In each of the wafers 10-17 there is provided a plurality of hourglass-shaped vias 25. Corresponding pyramid-shaped recesses 26 are normally provided in dummy wafer 18. In each of the vias 25 and recesses 26 there is provided a wad 27 of an electrically conductive compliant material, such as, for example, a fine wire or an electrically conductive elastomer. The vias 25 and recesses 26 in the wafers 10-18 are placed in registration with a corresponding via in an adjacent wafer, such that the wads 27 of electrically conductive compliant material in the vias combine to form a conductive vertical column providing electrical connections from feedthrough pins 22 to each of said semiconductor wafers 10-18.

While the embodiment of Fig. 1 shows a sealed housing 2, it is understood that conventional ports for circulating cooling gases or fluids may be added to the housing 2 in a manner as best fits the heat flow requirements of the application circuits located therein. Also, in certain applications, certain of the vias 25 may provide vertical connections between two or more but less than all of the wafers.

Referring to Figs. 2-11, the steps used for fabricating each of the semiconductive wafers in the stack of wafers 10-18 will now be described. For convenience, the description will be made with respect to wafer 10, it being understood that the other wafers 11-17, except for possible differences in the electrical circuits provided therein, are substantially identical insofar as the present invention is concerned.

Referring to Figs. 2 and 3, wafer 10, a 1,0,0 silicon wafer, is provided with a first or topside surface 30 and a second or backside surface 31. Electrical circuits, e.g. logic circuits, memory cells, or the like (not shown), are provided in the surface 30 and laterally electrically connected to one or more ring-shaped pads 32-37. While only 6 pads are shown, it is to be understood that many such pads are normally present on each wafer.

The surfaces 30 and 31 of the wafer 10 are then provided with a coating 34 of etch-resistant material such as silicon nitride as shown in Fig. 4. After the wafer 10 has been coated with the etch-resistant material, the coating 34 is patterned on the backside 31 of the wafer 10 by techniques known in the microlithographic art and plasma-etched so as to provide square openings 35 in the nitride coating

Claims

1. A semiconductor wafer array characterised in that it includes a plurality of wafers (10-18) of semiconductive material which are stacked one on top of another, each of the wafers (10-18) having at least one via (25) which is in alignment with a via (25) in an adjacent wafer (10-18), the via (25) having a first end terminated by a first hole (41) in a first surface (30) of the wafer (10), a second end terminated by a second and relatively larger hole (42) in a second and opposite surface (31) of the wafer, and a constriction in the via (25) between the first (41) and the second ends (42); insulation means (40) for electrically insulating the exposed surface of the via between the first (41) and said second ends (42); an electrically conductive pad (33) surrounding the first hole (41) for making an electrical connection to electrical circuits located on the first surface (30); and an electrically conductive compliant material which is located in the via (25) and, when not compressed, extends outwardly beyond the plane of the first (41) and said second holes (42) for making an electrical connection with the electrically conductive compliant material in the via (25) located in the adjacent one of the plurality of wafers (10-18) when the adjacent wafer (11) is pressed against either the first (30) or the second surfaces (31).

2. An array according to claim 1 wherein the constriction in the vias (25) in each of the wafers (10-18) restricts movement of the compliant material in the vias (25) through the first hole (41) when pressure is applied to the compliant material in the direction of the first hole (41).

3. An array according to claims 1 or 2 wherein the electrically conductive compliant material includes a cone-shaped portion.

4. An array according to any preceding claim wherein the electrically conductive compliant material comprises an elongated portion having substantially parallel side portions which extend from the apex of the cone-shaped portion.

5. An array according to claims 1 or 2 wherein the via (25) includes a section where the side walls are the shape of a truncated pyramid.

6. An array according to claims 1,2 or 5 wherein the via (25) comprises an elongated portion having substantially parallel side walls which extend from the truncated end of the pyramid-shaped side walls.

7. An array according to any preceding claim wherein the compliant material comprises a wad (27) of wire.

8. An array according to any of claims 1 to 6 wherein the compliant material comprises a compliant electrically conductive elastomer.

9. An array according to any preceding claim wherein the first surface (30) of each of the wafers (10-18) comprises a compliant electrically insulating material.

10. A semiconductor wafer array according to any preceding claim wherein the array further includes a housing (2) having base plate (3) and a top wall (7), the wafers (10-18) being stacked inside the housing (2) between and parallel to the base plate (3) and the top wall (7); a plurality of electrically conductive feed through pins (22) mounted in the base plate (3), so as to make electrical contact with the electrically conductive compliant material within the vias (25); and pressure means between the top wall (7) and the top wafer (18) to compress the wafers (10-18) and to produce an electrically conductive path between adjacent wafers (10-18).

11. An array according to claim 10 wherein the pressure applying means includes cooling means for conducting heat from stack of wafers (10-18) to the top wall (7).

12. An array according to claim 11 wherein the cooling means for conducting heat from the stack of wafers (10-18) to the top wall (7) comprises a compliant member (20) for compensating for thermal expansion and contraction of the stack of wafers (10-18).

13. An array according to claims 11 or 12 including means mounted in the top wall (7) and extending outwardly therefrom for dissipating heat from the top wall (7).

14. A method of making a semiconductor wafer array comprising the steps of: providing a plurality of wafers (10-18) of semiconductive material, each of the wafers (10-18) having a first (30) and a second surface (31) with an electrical circuit including an electrically conductive pad (32-37) having a central hole located on the first surface (30); providing a first hole having an inwardly directed side wall extending from the second surface (31) toward the first surface (30) in each of the wafers (10-18) beneath the pad (32-37); removing portions of the wall of the first hole for providing a second hole which diverges from the first hole to the edges of central hole of the pad (32-37) on the first surface (30) the first and said second holes combining to form a via (25); providing an electrically insulating layer (40) on the exposed wall surfaces of the via (25) in each of the wafers (10-18); inserting in each of the vias (25) produced by the exposing steps an electrically conductive compliant material, the material extending, when not compressed, beyond the plane of the ends of the vias (25); stacking the wafers one on top of the other so that the compliant material in a via (25) in one of the wafers (10-18) is in registration with the compliant material in the via (25) in an adjacent wafer (10-18); and compressing the adjacent wafers (10-18) together so as to compress the compliant material therebetween and thereby form an electrical circuit between the compliant material in the adjacent wafers (10-18).

15. A method of making a semiconductor wafer array comprising the steps of: providing a

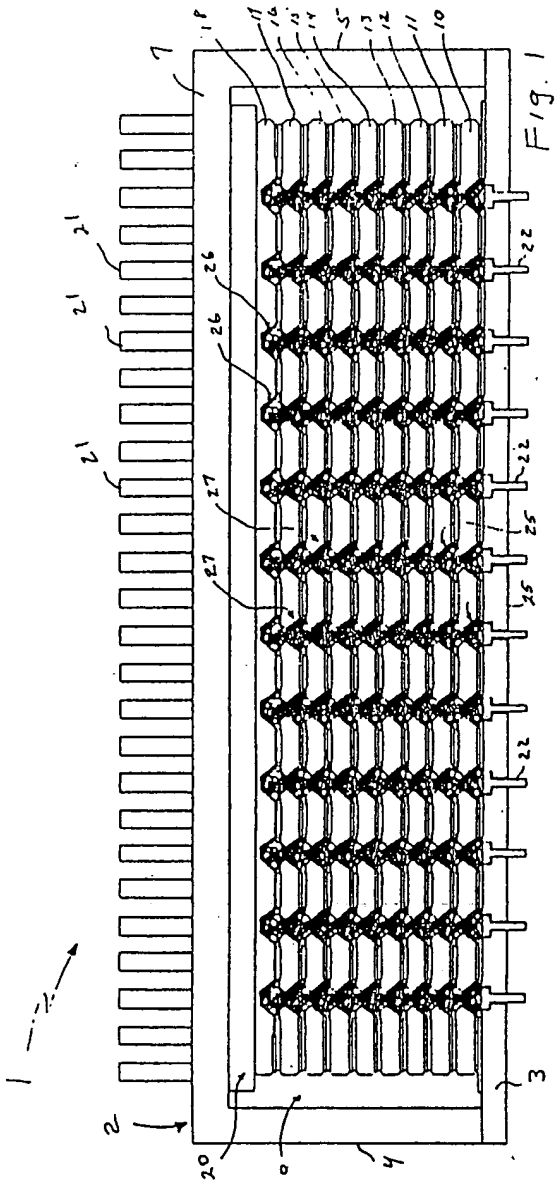


Fig. 1

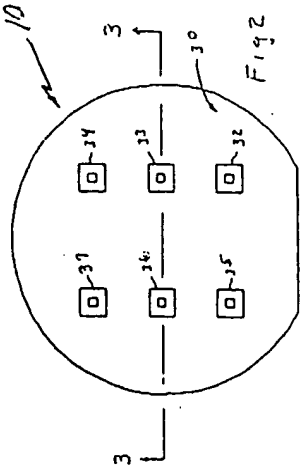


Fig. 2

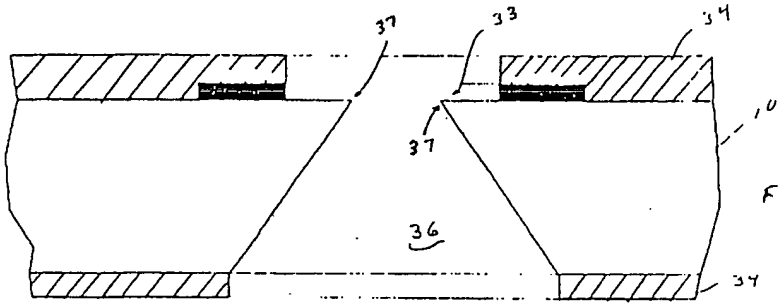


Fig 7

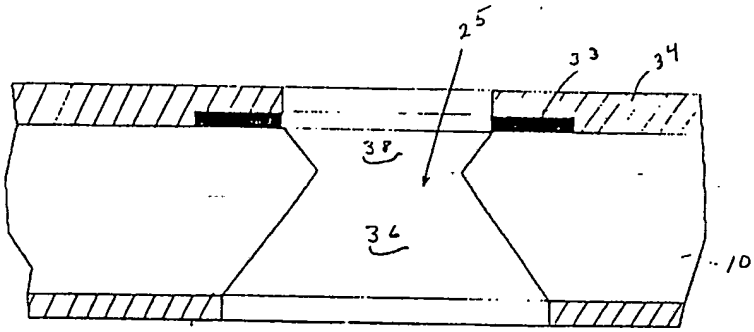


Fig 8

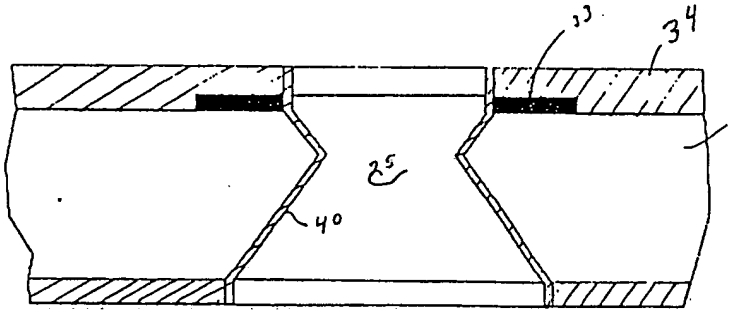


Fig 9

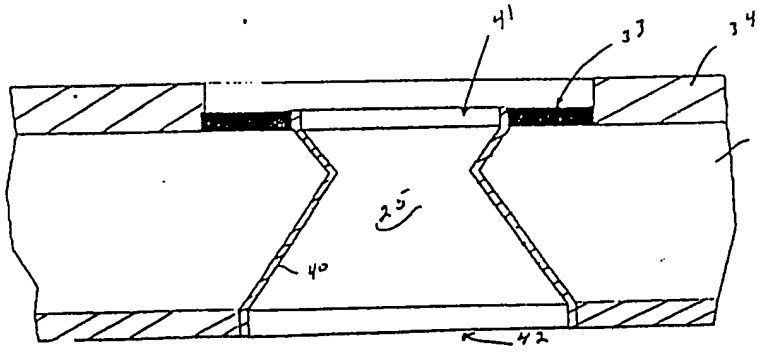


Fig 10

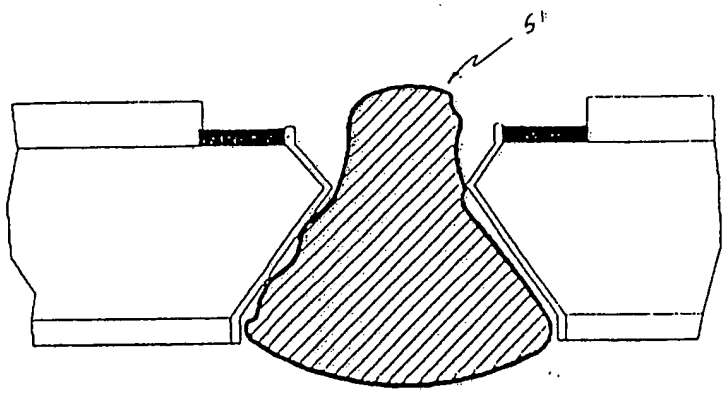


Fig 13

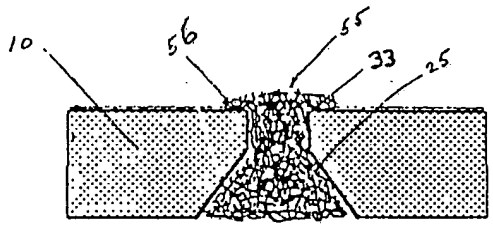
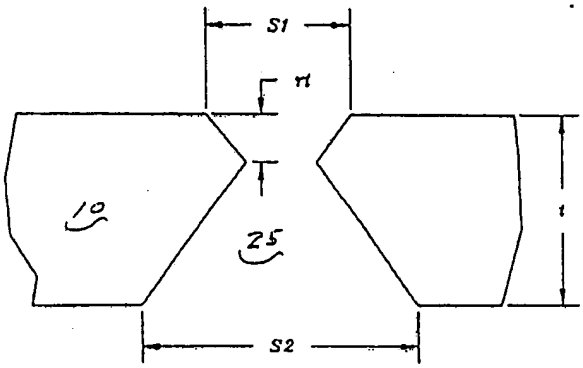


Fig. 14



$$S2 = S1 + \sqrt{2}\,t - 2\sqrt{2}\,rt$$

Fig 15